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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/057,154	01/25/2002	Kurt Gross	GR 01 P 0922	2489

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EXAMINER
WILLIAMS, ALEXANDER O

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 08/05/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/057,154	GROSS ET AL.
	Examiner	Art Unit
	Alexander O Williams	2826

-- Th MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Peri d for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 July 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

Serial Number: 10/057154 Attorney's Docket #: GR01P0922
Filing Date: 1/25/02; claimed foreign priority to 1/25/01

Applicant: Gross et al.

Examiner: Alexander Williams

Applicant's RCE in Paper # 13, filed 7/10/03 has been acknowledged.

Applicant's Amendment in Paper # 11, filed 6/10/03 has been acknowledged.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

Given the teaching of the references, it would have been obvious to determine the optimum thickness, temperature as well as condition of delivery of the layers involved. See *In re Aller, Lacey and Hall* (10 USPQ 233-237) "It is not inventive to discover optimum or workable ranges by routine experimentation. Note that the specification contains no disclosure of either the critical nature of the claimed ranges or any unexpected results arising therefrom. Where

patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. *In re Woodruff*, 919 f.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Claims 1, 2 and 6 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Baba (Japan Patent # 58-164232) in view of Camus et al.(EP # 0701281 A2).

For example, in claim 1, Baba et al. **(figures 1 to 4)** specifically figure 4 show a carrier **27** and a chip **20** configuration, comprising: a carrier **27** having a metal area essentially composed of copper; a chip **10** having a rear side metallization layer **25**; a buffer layer **26** configured on said metal area, said buffer layer being substantially composed of nickel; and a connection medium **17** for fixedly connecting said chip to said carrier; said chip being configured, without a chip housing, on said metal area such that only said connecting medium is configured between said rear side metallization layer of said chip and said buffer layer. Baba et al. explicitly fail to show the buffer layer being substantially composed of nickel and having a thickness between 5 to 10 micrometers.

Camus et al. is cited for showing a metallic coating for electrical chip boards. Specifically, Camus et al. discloses using a coating for an electrical chip board consisting of a Ni (alloy), a Au (alloy) layer on a substrate made of copper, having the Ni (alloy) layer having a thickness of 1-10 micro-meters for the purpose of reducing content enabling considerable cost savings.

In claim 2, the combination with Camus et al.' buffer layer has a thickness between 7 to 9 micrometers.

In claim 6, both references uses a carrier that is substantially composed of copper.

Therefore, it would be obvious to one of ordinary skill in the art at the time of the invention to use Camus et al.'s thickness of the Ni layer to modify Baba's Ni layer for the purpose of reducing content enabling considerable cost savings.

Claims 1 to 4 and 6 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Schneegans et al. (U.S. Patent # 5,901,901) in view of Camus et al. (EP # 0701281 A2).

For example, in claim 1, Schneegans et al. **(the figure show the structure, but the prior art discusses the claimed structure)** show a carrier and a chip configuration, comprising: a carrier **2** having a metal area essentially composed of copper; a chip **1** having a rear side metallization layer **3**; a buffer layer **4** configured on said metal area, said buffer layer being

substantially composed of nickel; and a connection medium **5** for fixedly connecting said chip to said carrier; said chip being configured, without a chip housing, on said metal area such that only said connecting medium is configured between said rear side metallization layer of said chip and said buffer layer (see column 1, lines 9-57). Schneegans et al. fail to explicitly show the buffer layer being essentially composed of nickel and having a thickness between 5 to 10 micrometers

Camus et al. is cited for showing a metallic coating for electrical chip boards. Specifically, Camus et al. discloses using a coating for an electrical chip board consisting of a Ni (alloy), a Au (alloy) layer on a substrate made of copper, having the Ni (alloy) layer having a thickness of 1-10 micro-meters for the purpose of reducing content enabling considerable cost savings.

In claim 2, the combination with Camus et al.' buffer layer has a thickness between 7 to 9 micrometers.

In claims 3 and 4, the combination with Schneegans et al.'s rear side metallization layer **3** is substantially composed of aluminum.

In claim 6, both references uses a carrier that is substantially composed of copper.

Therefore, it would be obvious to one of ordinary skill in the art at the time of the invention to use Camus et al.'s thickness of the Ni layer to modify Schneegans et al.'s Ni layer for the purpose of reducing content enabling considerable cost savings.

Claims 1, 2, 5 and 6 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Huang et al. (U.S. Patent Application Publication # 2002/0074672 A1) in view of Camus et al. (EP # 0701281 A2).

Initially, it is noted that the 35 U.S.C. § 103 rejection based on the buffer layers, connection medium and a metallization layer deals with an issue (i.e., the integration of multiple pieces into one piece or conversely, using multiple pieces in replacing a single piece) that has been previously decided by the courts.

In Howard v. Detroit Stove Works 150 U.S. 164 (1893), the Court held, "it involves no invention to cast in one piece an article which has formerly been cast in two pieces and put together...."

In In re Larson 144 USPQ 347 (CCPA 1965), the term "integral" did not define over a multi-piece structure secured as

a single unit. More importantly, the court went further and stated, "we are inclined to agree with the solicitor that the use of a one-piece construction instead of the [multi-piece] structure disclosed in Tuttle et al. would be merely a matter of obvious engineering choice" (bracketed material added). The court cited In re Fridolph for support.

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In re Fridolph 135 USPQ 319 (CCPA 1962) deals with submitted affidavits relating to this issue. The underlying issue in In re Fridolph was related to the end result of making a multi-piece structure into a one-piece structure. Generally, favorable patentable weight was accorded if the one-piece structure yielded results not expected from the modification of the two-piece structure into a single piece structure.

For example, in claim 1, Huang et al. **(5A to 5G)** specifically figure 5E show a carrier and a chip configuration, comprising: a carrier **11** having a metal area substantially composed of copper; a chip **1** having a rear side metallization layer **2**; a buffer layer **14** configured on said metal area, said buffer layer being substantially composed of nickel; and a connection medium **14** for fixedly connecting said chip to said carrier; said chip being configured, without a chip housing, on said metal area such that only said connecting medium is configured between said rear side metallization layer of said chip and said buffer layer (see column 1, lines 9-57). Schneegans et al. fail to explicitly show the buffer layer being essentially composed of nickel and having a thickness between 5 to 10 micrometers

Camus et al. is cited for showing a metallic coating for electrical chip boards. Specifically, Camus et al. discloses using a coating for an electrical chip board consisting of a Ni (alloy), a Au (alloy) layer on a substrate made of copper, having the Ni (alloy) layer having a thickness of 1-10 micro-meters for the purpose of reducing content enabling considerable cost savings.

In claim 2, the combination with Camus et al.'s buffer layer has a thickness between 7 to 9 micrometers.

In claim 5, the combination Huang et al.'s buffer layer **14** has a surface facing said chip, and said surface facing said chip, and said surface facing said chip includes a protective layer that is essentially composed of gold **[paragraph 0030].**

In claim 6, both references uses a carrier that is substantially composed of copper.

Therefore, it would be obvious to one of ordinary skill in the art at the time of the invention to use Camus et al.'s thickness of the Ni layer to modify Huang et al.'s Ni layer for the purpose of reducing content enabling considerable cost savings.

Therefore, it would have been obvious to one of ordinary skill in the art to use the buffer layers, connection medium and a metallization layer as "merely a matter of obvious engineering choice" as set forth in the above case law.

Claim 7 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Baba (Japan Patent # 58-164232) in view of Camus et al. (EP # 0701281 A2) and further in view of Arakawa et al. (U.S. Patent # 4,497,875).

The combination of Baba and Camus et al. show the features of the claimed invention as detailed above, but fail to explicitly show carrier includes a plate made of ceramic, said metal area is applied on said plate, and said metal area forms a contact area for said chip.

Arakawa et al. is cited for showing a ceramic substrate with metal plate. Specifically, Arakawa et al. (figures 1 to 4) specifically figure 4 discloses a show a carrier and a chip configuration, comprising: a carrier **1** having a metal area substantially composed of copper **21**; wherein carrier includes a plate made of ceramic, said metal area is applied on said plate, and said metal area forms a contact area for a chip; a chip **731,711** having a rear side metallization layer **713**; a buffer layer **81** configured on said metal area, said buffer layer being substantially composed of nickel; and a connection medium **61** for fixedly connecting said chip to said carrier; said chip being configured, without a chip housing, on said metal area such that only said connecting

medium is configured between said rear side metallization layer of said chip and said buffer layer for the purpose of reducing the heat dissipation resistance so as to increase the capacity of a hybrid integrated circuit.

Therefore, it would be obvious to one of ordinary skill in the art at the time of the invention to use Arakawa et al.'s ceramic and metal carrier in the combination of Camus et al.'s thickness of the Ni layer to modify Baba et al.'s Ni layer for the purpose of reducing the heat dissipation resistance so as to increase the capacity of a hybrid integrated circuit.

Claim 7 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Schneegans et al. (U.S. Patent # 5,901,901) in view of Camus et al. (EP # 0701281 A2) and further in view of Arakawa et al. (U.S. Patent # 4,497,875).

The combination of Schneegans et al. and Camus et al. show the features of the claimed invention as detailed above, but fail to explicitly show carrier includes a plate made of ceramic, said metal area is applied on said plate, and said metal area forms a contact area for said chip.

Arakawa et al. is cited for showing a ceramic substrate with metal plate. Specifically, Arakawa et al. (figures 1 to 4) specifically figure 4 discloses a show a carrier and a chip configuration, comprising: a carrier **1** having a metal area substantially composed of copper **21**; wherein carrier includes a plate made of ceramic, said metal area is applied on said plate, and said metal area forms a contact area for a chip; a chip **731,711** having a rear side metallization layer **713**; a buffer layer **81** configured on said metal area, said buffer layer being substantially composed of nickel; and a connection medium **61** for fixedly connecting said chip to said carrier; said chip being configured, without a chip housing, on said metal area such that only said connecting medium is configured between said rear side metallization layer of said chip and said buffer layer for the purpose of reducing the heat dissipation resistance so as to increase the capacity of a hybrid integrated circuit.

Therefore, it would be obvious to one of ordinary skill in the art at the time of the invention to use Arakawa et al.'s ceramic and metal carrier in the combination of Camus et al.'s thickness of the Ni layer to modify Schneegans et al.'s Ni layer for the purpose of reducing the heat dissipation resistance so as to increase the capacity of a hybrid integrated circuit.

Claim 7 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Huang et al. (U.S. Patent Application Publication # 2002/0074672 A1) in view of Camus et al. (EP # 0701281 A2) and further in view of Arakawa et al. (U.S. Patent # 4,497,875).

The combination of Huang et al. and Camus et al. show the features of the claimed invention as detailed above, but fail to explicitly show carrier includes a plate made of ceramic, said metal area is applied on said plate, and said metal area forms a contact area for said chip.

Arakawa et al. is cited for showing a ceramic substrate with metal plate. Specifically, Arakawa et al. (figures 1 to 4) specifically figure 4 discloses a show a carrier and a chip configuration, comprising: a carrier **1** having a metal area substantially composed of copper **21**; wherein carrier includes a plate made of ceramic, said metal area is applied on said plate, and said metal area forms a contact area for a chip; a chip **731,711** having a rear side metallization layer **713**; a buffer layer **81** configured on said metal area, said buffer layer being substantially composed of nickel; and a connection medium **61** for fixedly connecting said chip to said carrier; said chip being configured, without a chip housing, on said metal area such that only said connecting medium is configured between said rear side metallization layer of said chip and said buffer layer for the purpose of reducing the heat dissipation resistance so as to increase the capacity of a hybrid integrated circuit.

Therefore, it would be obvious to one of ordinary skill in the art at the time of the invention to use Arakawa et al.'s ceramic and metal carrier in the combination of Camus et al.'s thickness of the Ni layer to modify Huang et al.'s Ni layer for the purpose of reducing the heat dissipation resistance so as to increase the capacity of a hybrid integrated circuit.

Any differences in the claimed invention and the prior art may be expected to result in some differences in properties. The issue is whether the properties differ to such an extent that the difference is really unexpected. *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986)

Appellants have the burden of explaining the data in any declaration they proffer as evidence of non-obviousness. *Ex parte Ishizaka*, 24 USPQ2d 1621, 1624 (Bd. Pat. App. & Inter. 1992).

An Affidavit or declaration under 37 CFR 1.132 must compare the claimed subject matter with the closest prior art to be effective to rebut a prima facie case of obviousness. *In re Burckel*, 592 F.2d 1175, 201 USPQ 67 (CCPA 1979).

Field of Search	Date
U.S. Class and subclass: 257/703,700,701,702,676,765,763,766,769,758,771-773,762 156/278	8/26/02 3/7/03 7/27/03
Foreign Documentation: foreign patents and literature in 257/703,700,701,702,676,765,763,766,769,758,771-773,762 156/278	8/26/02 3/7/03 7/27/03
Electronic data base(s): U.S. Patents EAST	8/26/02 3/7/03 7/27/03

Papers related to this application may be submitted to Technology Center 2800 by facsimile transmission. Papers should be faxed to Technology Center 2800 via the Technology Center 2800 Fax center located in Crystal Plaza 4-5B15. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Technology Center 2800 Fax Center number is (703) 308-7722 or 24. Only Papers related to Technology Center 2800 APPLICATIONS SHOULD BE FAXED to the GROUP 2800 FAX CENTER.

Any inquiry concerning this communication or any earlier communication from the examiner should be directed to ***Examiner Alexander Williams*** whose telephone number is **(703) 308-4863**.

Any inquiry of a general nature or relating to the status of this application should be directed to the ***Technology Center 2800 receptionist*** whose telephone number is **(703) 308-0956**.

7/28/03

Primary Examiner
Alexander O. Williams